In the Specification

Please replace the paragraph on page 38, lines 11-14 with the following markup paragraph:

According to one embodiment, the cache line size has been increased to 64 bytes (the cache line size in some Pentium® processors is 32 bytes.). Thus, using the quad pumped signaling protocol and a data bus width of ~~with~~ 64 data lines, a cache line (or 64 bytes) can be transmitted or transferred in two bus clock cycles:
